REMARKS

Claim Rejections – 35 U.S.C. §103

Claims 1-3 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Abramovici et al. (US 6,108,806), in view of Andrews et al. (US 6,064,225), in further view of Kean (US 6,292,018).

For a §103 obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. MPEP 2143.

Claim 1 recites "a method of testing the routing circuitry in a field programmable gate array (FPGA) having a first FPGA tile, said routing circuitry having a first set of tracks having first and second ends, and a second set of tracks having first and second ends and intersecting said first set of tracks, said second set of tracks used to route the internal signals of the FPGA, said routing structure having programmable interconnect elements at selected intersections of said first set of tracks and said second set of tracks, ... wherein said first FPGA tile comprises a plurality of interface groups (IGs), each of said IGs having a plurality of input multiplexers configurable to select signals received from outside of said FPGA tile and provide signals to said routing circuitry inside said FPGA tile, and a plurality of input/output pads (I/Os) coupled to at least one of said input multiplexers of at least one of said IGs."

Abramovici fails to disclose the method of Claim 1, wherein the first FPGA tile comprises a plurality of interface groups (IGs), each of the IGs having a plurality of input multiplexers configurable to select signals received from outside of the FPGA tile and provide signals to the routing circuitry inside the FPGA tile, and a plurality of input/output pads (I/Os) coupled to at least one of the input multiplexers of at least one of the IGs. On Page 3 of the Office Action dated November 16, 2005, Examiner even admits that Abramovici fails to disclose these limitations. However, Examiner asserts that Andrews teaches these limitations and that it would have been obvious to one ordinarily skilled in the art to modify Abramovici's invention to include these additional components taught in Andrews, arguing that the motivation would be to enable Abramovici to selectively route signals from outside of the FPGA to the PLCs and other programmable logic blocks. Applicant respectfully disagrees with Examiner's assertion.

According to MPEP 2145(X)(D)(2), it is improper to combine references where the references teach away from their combination.

Abramovici discusses the shortcomings of the prior art, stating that the "first test method, disclosed in U.S. Pat. No. 6,003,150, utilizes significant amounts of global routing." (Col. 1, lines 50-52). Abramovici teaches away from the addition of components to enable more routing, stating that it improves upon the prior art "by providing a new, hybrid method that utilizes only a very limited amount of global routing to provide complete diagnostic testing of an FPGA ...." (Col. 1, lines 59-64).

Since Abramovici teaches away from the expansion of routing, it teaches away from the combination suggested by Examiner. Therefore, one skilled in the art would not be motivated to modify Abramovici to include the additional components taught in Andrews. Applicant respectfully submits that Examiner has failed to establish that the prior art relied upon, coupled with knowledge generally available in the art at the time of

the invention, contains some suggestion or incentive that would have motivated the skilled artisan to modify the references as suggested by Examiner.

Therefore, Applicant respectfully submits that Claim 1 is non-obvious over Abramovici in view of Andrews, in further view of Kean, and that Claim 1 is currently in condition for allowance.

The same arguments made above with respect to the patentability of Claim 1 are applicable to the patentability of Claims 2 and 3 as well. Applicant respectfully submits that Claims 2 and 3 are currently in condition for allowance.

Reconsideration and withdrawal of this rejection is respectfully requested.

Claims 4 and 5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Abramovici, in view of Wells et al. (US 6,651,238), in further view of Andrews, in even further view of Kean.

The same arguments made above with respect to the patentability of Claim 1 are applicable to the patentability of Claim 4 as well.

Since Claim 5 depends from Claim 4, Applicant respectfully submits that Claim 5 is also patentable as it contains the same limitations as Claim 4.

Applicant respectfully submits that Claims 4 and 5 are currently in condition for allowance. Reconsideration and withdrawal of this rejection is respectfully requested.

If the Examiner has any questions regarding this application, the Examiner may telephone the undersigned at 775-586-9500.

Respectfully submitted,
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